

REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1-3, 19 and 20 are rejected. Claims 1-3, 19 and 20 are amended. Claims 1-20 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102(a)

It is asserted in the Office Action that claims 1-3, 19-20 are rejected under 35 U.S.C. § 102(a), as being anticipated by Applicant Admitted Prior Art (AAPA). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

[a] semiconductor device for comparing an input address with a stored repair address, comprising: a signal controller for generating control signals and an enable signal; an address latch unit in response to the control signals for latching the input address; N number of M-bit address comparators, each for comparing the latched input address with the stored repair address in response to a fuse reset signal and the enable signal; a comparator delay modeling block for delaying the enable signal for a predetermined time; and a repair circuit controller in response to the delayed enable signal output from the comparator delay modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators.

Applicant's amended claim 19 contains the limitations of

[a] semiconductor device for comparing an input address with a stored repair address, comprising: a signal controller for generating control signals and an enable signal; an address latch unit in response to at least one of the control signals for latching the input address; N number of M-bit address comparators, each for comparing the latched input address with the stored repair address in response to a fuse reset signal and the enable signal; a comparator delay modeling block for delaying the enable signal for a predetermined time; a repair circuit controller in response to the delayed enable signal output from the comparator delay modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators; and a comparator initialization unit for initializing the N number of M-bit address comparators.

AAPA does not disclose, teach or suggest N number of M-bit address comparators, each for comparing a latched input address with a stored repair address in response to a fuse reset signal and an enable signal output from signal controller. It is asserted in the Office Action that signal AE of AAPA corresponds to an enable signal RAE_FUSE of the Applicant's claimed invention. AAPA's AE signal, however, is only an input to an address latch unit 40. Therefore, the address comparators 10 of AAPA only receive the latched input address RAZ<2:M-1> and a reset signal FUSE_RESET. Distinguishable, the enable signal RAE_FUSE of Applicant's claimed invention is input to a plurality of repair address comparators 100 and a repair comparison replica 700. That is, the address comparators 100 of Applicant's claimed invention receives the latched input address RAZ<2:M-1>, a reset signal FUSE_RESET and the enable signal RAE_FUSE. Accordingly, the address comparators 100 of Applicant's claimed invention are absolutely different from those of AAPA.

Therefore, since AAPA does not disclose, teach or suggest all of Applicant's amended claims 1 and 19 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(a) has not been adequately set forth relative to AAPA. Thus, Applicant's amended

claims 1 and 19 are not anticipated by AAPA. Additionally, the claims that directly or indirectly depend on amended claims 1 and 19, namely claims 2-3, and 20, respectively, are also not anticipated by AAPA for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(a) rejections for claims 1-3 and 19-20 are respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 4-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-20, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: November 6, 2006

By: _____

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on November 6, 2006.

Jean Svoboda